## REMARKS

Claims 21 - 37 were pending in the application. Claims 21, 30, 32, and 36 have been amended. Accordingly, Claims 21-37 remain pending in the application.

Support for claims 21, 30, 32, and 36 may be found, for example, on page 12, line 1 – page 13, line 2 of the disclosure.

The Examiner objected to the drawings. Applicant has corrected the drawings to overcome this objection.

## 35 U.S.C. §102 Rejections

Claims 21-37 were rejected under 35 U.S.C. §102(b) as being anticipated by Kobasyashi et al. (GB 2,290,891).

Applicant discloses, on page 11, lines 20-25 of Applicant's Specification,

> "Embodiments of the present invention provide an arrangement in which the version register or at least the part of the version register which contains the processor identification is made to be read/writeable, and to write into the version register a predefined value which is common to all processors within the computer system. As a result the false detection of an error in the system is prevented or at least the likelihood of a false detection of an error reduced."

In addition, the Applicant further discloses, on page 12, lines 2-29,

> "The read/writeable register 64 forms the version identification register, and is arranged to receive the contents of the read only register 62 under control of a control unit 66 via the internal bus 71...In operation on power-up, the contents of the read only register 62 are written under control of the control unit 66 into a writeable part 94 of the version identification register 64. In this mode therefore the manufacturer's version identification data identifying the processor, the implementation identification and the mask set version, for example, are loaded into the corresponding field or fields of the version identification register 64. According to the example present in the table shown in Figure 5, the version identification register 64 may contain other configuration information such as MAXTL and MAXWIN, which may be loaded permanently in a read only section

> 92 of the register 64, as will be explained shortly...In this embodiment, the read/writeable version register 64 is divided into two parts, with the first part 92 containing information appertaining to the configuration of the processor 52...The first part 92 of the version register 64 is made to be a read only part and so is not overwritten by either the information from the read only register 62 or the common predefined value written into the second part 94 of version register 64 which is loaded from the bus 54 via the internal bus 71." (Emphasis added)

Kobasyashi teaches a method for initializing a multiprocessor system while resetting defective CPU's detected during operation. Specifically, Kobasyashi teaches "an identifier setting register, connected to the common bus, capable of assigning to and reading from an arbitrary CPU a CPU number, for designating assigned CPU numbers to the respective CPUs." (Kobasyashi, Page 8, Lines 9-12) Also, Kobasyashi teaches "the identifier setting register designates the CPU numbers in the predetermined order only to normal CPUs; the reset controller cuts off defective CPUs from the common bus." (Kobasyashi, Page 9, Lines 11-13)

Applicant respectfully submits that Kobasyashi fails to teach or suggest "wherein each of said processors comprises a processor identification register comprising: a first field which is read/writeable and which is configured to store data representative of a processor version of the processor; and a second field which is configured to store data representative of a configuration of the processor, wherein each of said processors being configured, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said first field of its processor identification register" as recited in claim 21. Applicant respectfully submits that Kobayashi fails to teach a processor identification register having more than one field. In particular, Kobayashi et al is silent with regard to **a first field** which is read/writable and which is configured to store data representative of a *processor version* of the processor. Kobayashi et al is also silent with regard to a processor identification register including **a second field** which is configured to store data representative of a *configuration* of the processor.

In accordance, claim 21 is believed to patentably distinguish over Kobasyashi.

Claims 22-29 depend on claim 21 and are therefore believed to patentably distinguish over Kobasyashi for at least the reasons given above.

Applicant respectfully submits that Kobasyashi fails to teach or suggest "a processor identification register coupled to said interface, said register comprises: a first field which is read/writeable and which is configured to store data representative of a processor version of the processor; and a second field which is configured to store data representative of a configuration of the processor, wherein said processor is responsive to a masking condition, to write a common predefined data value received via said I/O bus into said first field of said processor identification register, wherein said predefined data value is common to said processing sets and is operable to mask said data representative of a processor version" as recited in claim 30. In accordance, claim 30 is believed to patentably distinguish over Kobasyashi.

Claim 31 depends on claim 30 and is therefore believed to patentably distinguish over Kobasyashi for at least the reasons given above.

Applicant respectfully submits that Kobasyashi fails to teach or suggest "wherein at least a first processor in said computer system comprising a processor identification register comprising: a first field which is read/writeable and which is configured to store data representative of a processor version of the processor; and a second field which is configured to store data representative of a configuration of the processor, said method comprising: detecting a predetermined condition representative of a state in which a processor identification is present in the processor identification register of said first processor; and loading a common predefined data value into said first field of processor identification register of said first processor, which predefined data value is common to said processing sets and is operable to mask said processor version" as recited in claim 32. In accordance, claim 32 is believed to patentably distinguish over Kobasyashi.

Claims 33-35 depend on claim 32 and are therefore believed to patentably distinguish over Kobasyashi for the same reasons.

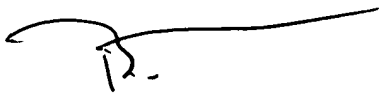
Applicant respectfully submits that Kobasyashi fails to teach or suggest "replacing the removed processor with a replacement processor that comprises: an interface for communication with an I/O bus, and a processor identification register comprising: a first field which is read/writeable and which has data representative of a processor version of the processor stored therein; and a second field which has data representative of a configuration of the processor stored therein, wherein said replacement processor is responsive to a masking condition, to write a common predefined data value received via said I/O bus into said first field of said processor identification register, wherein said predefined data value is common to said processing sets and is operable to mask data representative of a said processor version" as recited in claim 36. In accordance, claim 36 is believed to patentably distinguish over Kobasyashi.

Claim 37 depends on claim 36 and is therefore believed to patentably distinguish over Kobasyashi for the same reasons.

In light of the foregoing amendments and remarks, Applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If a phone interview would speed allowance of any pending claims, such is requested at the Examiner's convenience.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-80100/BNK.

Respectfully submitted,



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